

WE CLAIM:

1. A method for forming a MOS transistor gate dielectric layer comprising:

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providing a semiconductor substrate;

forming an oxide layer on the semiconductor substrate;

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exposing the oxide layer to a high-density nitrogen plasma to incorporate nitrogen into the oxide layer thereby converting the oxide layer to an oxynitride layer; and

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annealing said oxynitride layer in N_2O to form an oxynitride layer with a uniform nitrogen concentration profile.

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2. The method of claim 1 wherein the exposing the oxide layer to a high-density nitrogen plasma comprises a plasma power level of 700 - 900 watts.

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3. The method of claim 1 wherein annealing the oxynitride layer in N_2O comprises rapid thermal annealing at a temperature of $800^{\circ}C$ - $1100^{\circ}C$ for 10-60 seconds.

4. A method of forming a MOS transistor comprising:

5 providing a semiconductor substrate;

forming a gate dielectric layer on the
semiconductor substrate wherein the gate
dielectric layer has a uniform nitrogen
10 concentration;

forming a conductive layer on said gate
dielectric layer,

15 forming sidewall structures adjacent to said
conductive layer; and

forming source and drain regions in the
semiconductor substrate adjacent to said sidewall
20 structures.

5. The method of claim 4 wherein said forming a gate
dielectric layer with a uniform nitrogen concentration
comprises:

25 forming an oxide layer on the semiconductor
substrate;

30 exposing the oxide layer to a high-density
nitrogen plasma to incorporate nitrogen into the
oxide layer thereby converting the oxide layer to
an oxynitride layer; and

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11. A MOS transistor, comprising:

providing a silicon substrate;

a gate dielectric layer on the silicon substrate wherein the gate dielectric layer is less than 40 angstroms thick and wherein the gate dielectric layer has a uniform nitrogen concentration;

a conductive layer on the gate dielectric layer;

sidewall structures adjacent to said conductive layer; and

source and drain regions in the silicon substrate adjacent to the sidewall structures.

12. The MOS transistor of claim 10 wherein the uniform nitrogen concentration is greater than 6 atomic percent.

13. The MOS transistor of claim 12 wherein the uniform nitrogen concentration has a variation of less than 10% across the gate dielectric layer.

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